LANGER
EMV-Technik

Achieve interference immunity by identifying and eliminating EMC weak points :

Strategy with field sources - H2 set and H3 set Field Sources from Langer EMV-Technik GmbH and E1 set Immunity Development System.

Introduction

Field sources are essential tools for EMC immunity testing during development. They enable developers to pulse various surface areas of electronic assemblies with electric or magnetic fields in a targeted manner.

Normally, this type of pulsing is started with low-resolution field sources in order to influence larger areas of the assembly with widely distributed field bundles. This makes it possible to narrow down fault areas, but not to determine the exact causes of the faults. For this reason, higher resolution field sources are then used. These emit narrow and concentrated field beams, which can be used to clearly identify weak points within the fault areas.

Click here for more information:

SALES-PACK download

Co-funded by the European Union

This project is co-financed from tax revenues on the basis of the budget adopted by the Saxon State Parliament.

LANGER EMV-Technik GmbH
Nöthnitzer Hang 31
01728 Bannewitz
Germany

Using the Field Sources for Troubleshooting

A prerequisite is that the module is pulsed with a standard generator (ESD or burst) in accordance to the standard. The resulting fault patterns must be precisely recorded and must subsequently be found again during localization with field sources.

Note: During the analysis with field sources, new fault patterns are sometimes detected. These often occur below the interference threshold of the standard test and are therefore less critical. Later, these additional fault patterns can also be eliminated and thus contribute to the hardening of the assembly.

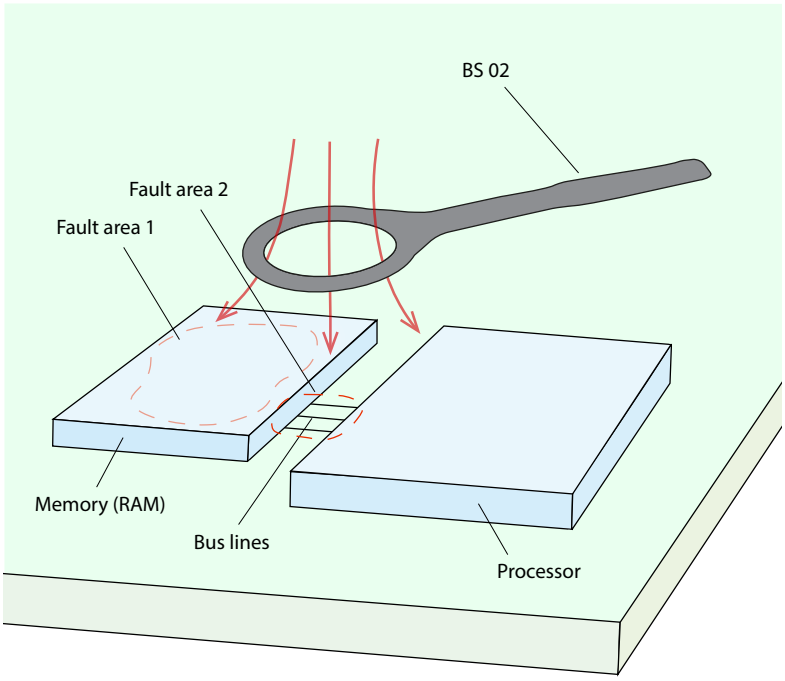

Figure 1 – Pulsing with BS 02 magnetic field source

Practical Example

Figures 1 to 3 show an electronic circuit in which a processor controls a screen via HDMI. The processor is connected to a memory circuit (RAM) via bus lines (Figure 1-3) and continuously retrieves its program code from this circuit.

The pulsing with a standard generator leads to the error pattern that the image content on the HDMI monitor freezes. The error can only be rectified by interrupting the power supply to the processor.

The first task is to reproduce the screen freezing error when the module is pulsed with field sources. The HDMI system (HDMI connector, cable, and monitor) is the first possible source of error to be considered.

Co-funded by the European Union

This project is co-financed from tax revenues on the basis of the budget adopted by the Saxon State Parliament.

LANGER EMV-Technik GmbH
Nöthnitzer Hang 31
01728 Bannewitz
Germany

Troubleshooting begins with the BS 02 magnetic field source, the largest magnetic field source in the E1 set immunity development system.

Alternatively, the BS 02-h from the H2/H3 field source set can be used in conjunction with a burst generator or the BS 02-h from the TS 23 set TroubleStar Development System for ESD / Burst.

The BS 02 is guided over the module at a maximum distance of two centimeters (Figure 1). The possible confinement of the weak point corresponds approximately to the size of the field source head.

When the HDMI system is pulsed with the field source, image interference or a black screen occurs, but this does not correspond to the error pattern being searched for. The entire module is then exposed to the BS 02 field source section by section. In the area of the processor and RAM, the fault being searched for can actually be reproduced.

With the higher resolution field source BS 04 DB (E1 set), the fault can be narrowed down further (Figure 2). Alternatively, BS 04DB-h from the field source sets H2 and H3 set can also be used in conjunction with a burst generator.

It is initially unclear whether the cause lies in the RAM, in the conductor lines or in the processor. The pulsing of the surface of the memory circuit generates new error images on the monitor (similar to a checkerboard pattern), which are not relevant for the time being (see above).

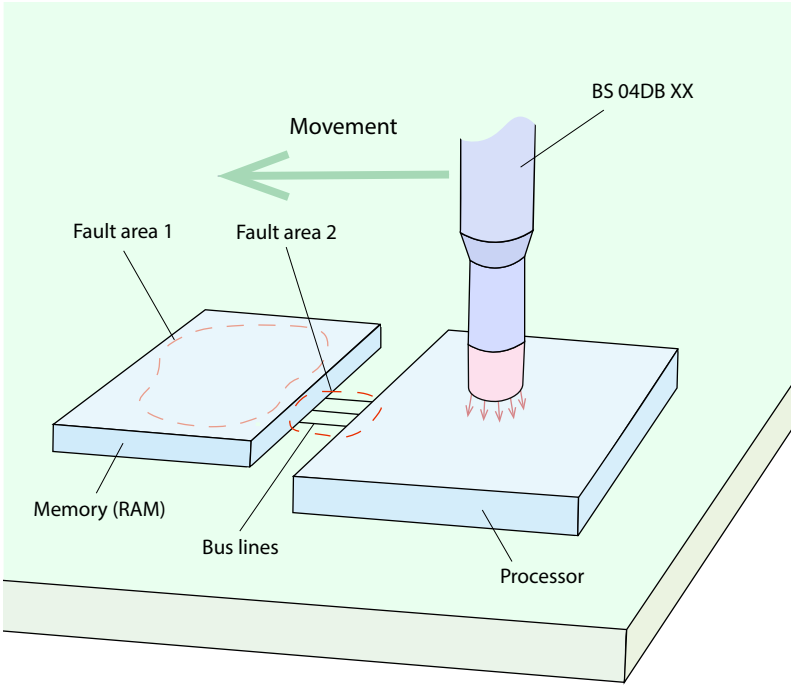

Figure 2 - Narrowing down the fault areas with BS 04 DB XX

Co-funded by the European Union

This project is co-financed from tax revenues on the basis of the budget adopted by the Saxon State Parliament.

LANGER EMV-Technik GmbH
Nöthnitzer Hang 31
01728 Bannewitz
Germany

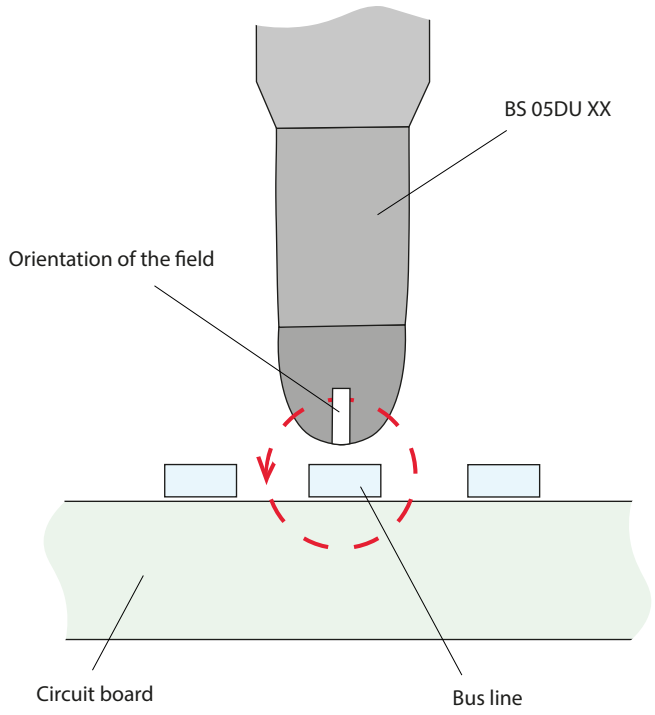

Figure 3 Pulsing of a bus line with BS 05DU XX

For further analysis, the area of the bus lines between the two ICs is examined with the BS 05 DU field source (Figure 3). Here the fault pattern can be reproduced directly on these lines.

With this knowledge, suitable countermeasures can now be tested.

To prevent interference on the bus lines, they must be shielded. As a test, the bus lines are therefore covered with copper foil and the module is pulsed with the standard generator again. The result is that the shielding prevents the corresponding error pattern.

The successful shielding can now be put into practice with appropriate layout measures. For example, the bus lines could be laid in an inner layer and shielded with a ground layer.

Note: This interference immunity test should be carried out as early as possible in the development phase (first prototype) in order to avoid unnecessary layout changes.

The targeted, strategic use of field sources provides developers with effective tools for identifying weak points in the design and then taking targeted countermeasures.

Use the following Langer EMV products for this purpose:

- E1 set Immunity Development System
- TS 23 set TroubleStar Development System for ESD / Burst
- H2 set and H3 set Field Sources

Co-funded by the European Union

This project is co-financed from tax revenues on the basis of the budget adopted by the Saxon State Parliament.

LANGER EMV-Technik GmbH
Nöthnitzer Hang 31
01728 Bannewitz
Germany

LANGER EMV-Technik

Coming soon

Troublestar TS 23

Application Practical example
ESD interference suppression

Introduction

In a world where microcontroller platforms are increasingly being integrated into modern technology solutions, the need for these devices to function reliably and interference-free is also increasing. Microcontroller platforms are used in areas such as education, home automation and industry due to their flexibility, adaptability and cost-effectiveness. Therefore, the electromagnetic compatibility (EMC) of these devices is crucial to ensure that they operate effectively under different environmental conditions without being affected by electromagnetic interference (EMI).

In our EMI suppression example, we investigate the effects of electrostatic discharge (ESD) on a microcontroller platform used as a control device in critical applications.

Click here for more information:

SALES-PACK download

Co-funded by the European Union

This project is co-financed from tax revenues on the basis of the budget adopted by the Saxon State Parliament.

LANGER EMV-Technik GmbH
Nöthnitzer Hang 31
01728 Bannewitz
Germany

Main Section

The ESD gun is a rather imprecise tool that exposes a large area of the assembly and does not allow the exact location of weak points. Rapid localization of specific weak points is virtually impossible, and a lot of time is spent on trial and error.

In our example, the tip of the ESD gun is placed on the RJ45 socket on the left-hand side of the device under test and the gun head is swung down onto the device under test. The ESD discharge triggers the following error pattern: the image on the monitor, which is connected via HDMI, freezes and the processor stops.

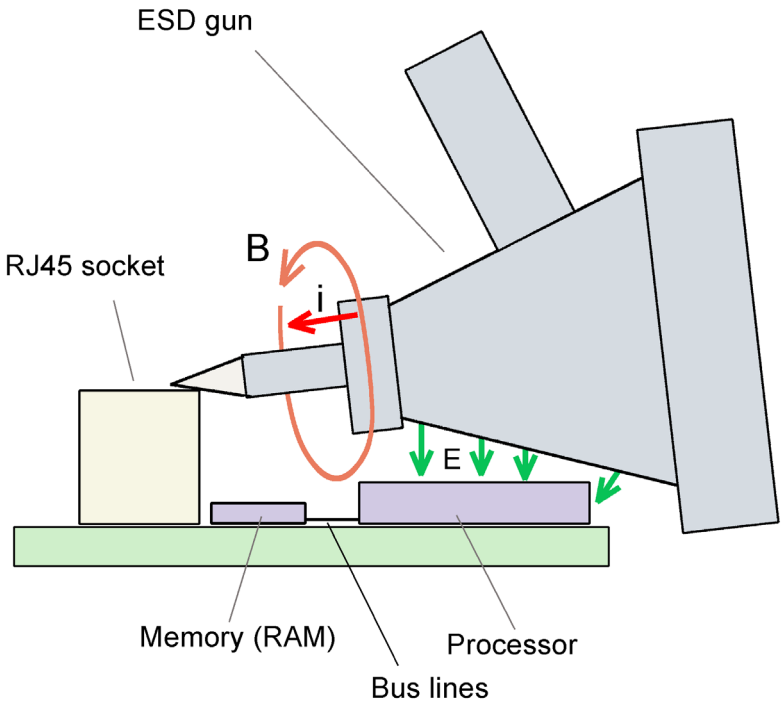

Figure 1 Interference from electrostatic discharge on a microcontroller platform

The processor only reactivates by interrupting the power supply. It can therefore be assumed that the processor is directly affected by the ESD process. The DE 2 differential coupler (Figure 2) is used to test this assumption.

Co-funded by the European Union

This project is co-financed from tax revenues on the basis of the budget adopted by the Saxon State Parliament.

LANGER EMV-Technik GmbH
Nöthnitzer Hang 31
01728 Bannewitz
Germany

A current is fed into the AB connection via the metal coating of the processor, which generates a magnetic field in the processor. With the BC connection, the voltage of the TS 23 Troublestar is applied to the processor against ground, generating an electrical ESD field.

The test shows that the processor operates faultlessly up to a voltage of 2.3 kV.

To further localize the fault, the differential magnetic field probe BS 04DB-d is used to search the processor area of the circuit board for the functional fault described above. The fault pattern can be reproduced in the area between the processor and the memory circuit. However, the BS 04DB-d field source has too low a resolution to clearly identify the fault location. For this reason, the BS 05 DU-h field source is used next. Due to the higher resolution, the bus lines can be determined as the exact weak point.

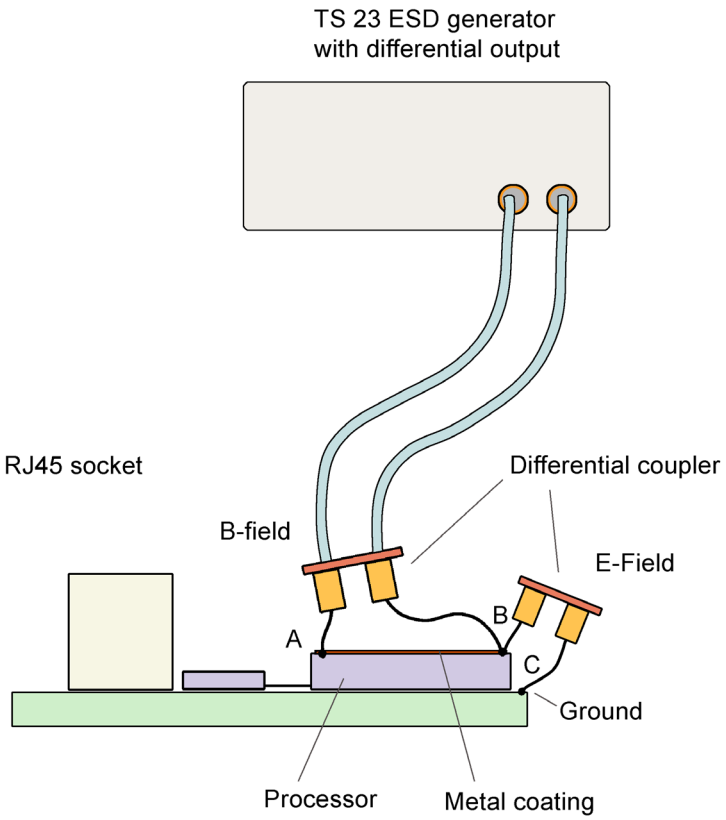

Figure 2 Using the DE 2 differential coupler and the TS 23 Troublestar to test the processor

Note: When the surface of the memory circuit was exposed, additional fault images such as the destruction of the image content of the HDMI display occurred. As the processor continued to run, these additional error patterns were not relevant.

Co-funded by the European Union

This project is co-financed from tax revenues on the basis of the budget adopted by the Saxon State Parliament.

LANGER EMV-Technik GmbH
Nöthnitzer Hang 31
01728 Bannewitz
Germany

Verifying the Cause

To confirm that the bus lines on the surface of the circuit board are the cause, these are covered with copper foil and thus shielded. Repeated exposure of the module to the ESD gun no longer leads to the fault pattern.

Countermeasures

A layout modification is required to permanently eliminate the problem. The bus cables should therefore be laid in an inner layer and shielded on the surface with ground planes.

The development of robust EMC test methods and solutions for microcontroller platforms is therefore not only a technical need, but also a prerequisite for ensuring reliability and functionality in an increasingly interconnected and technologically dependent world.

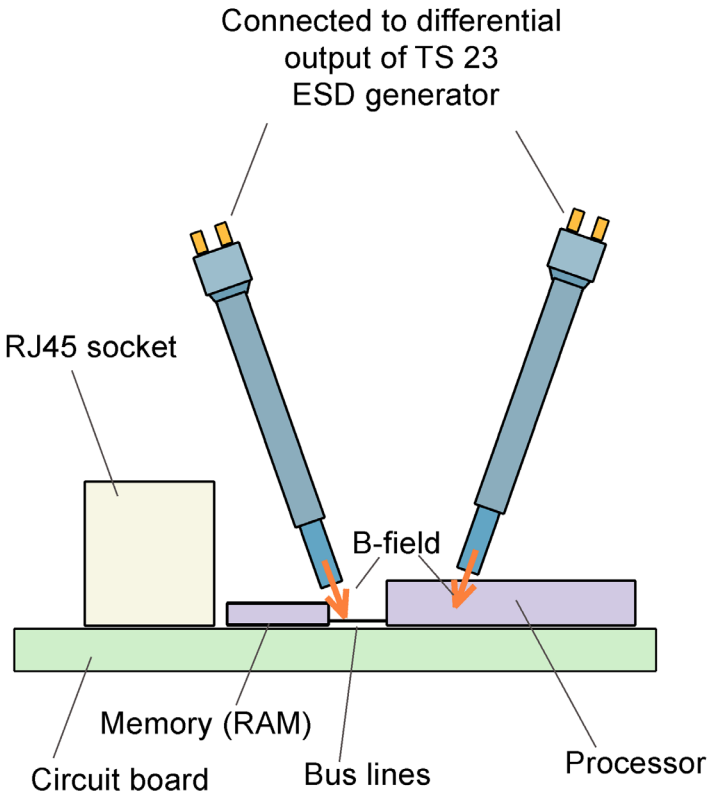

Figure 3 Pulsing with the magnetic field source to isolate ESD weak points on the surface of the circuit board

Mission

Langer EMV-Technik's mission is to enable our customers to develop their products efficiently and fault-free. We strive to increase development speed and maximize quality through innovative solutions and first-class support. Our goal is to enable our customers to enter the market with confidence, supported by our technologies and services.

Co-funded by the European Union

This project is co-financed from tax revenues on the basis of the budget adopted by the Saxon State Parliament.

LANGER EMV-Technik GmbH
Nöthnitzer Hang 31
01728 Bannewitz
Germany

Seminars

This is supported by the expertise our customers receive in our experimental seminars. These offer development engineers considerable added value. Both in the area of immunity and interference emission, we enable participants to directly understand EMC mechanisms of action at their own experimental station using practical examples. The Immunity Part 1 seminar focuses on pre-compliance measurements with the E1 set and field sources. It is common practice in the seminar for participants to describe their problems and receive support and advice on how to solve them. The knowledge gained can then be applied directly in their own work area. Further information can be found here: Langer EMV-Technik - Seminars

Consulting

For specific EMC problems, it may also be worth booking one or two days of consulting directly at our premises. Our EMC consulting engineers solve EMC problems and suppress interference in your electronic assemblies in the shortest possible time, both in the area of interference immunity and interference emission. The company's development team is involved in the process and all modifications and options are explained in detail and the implementation and success are verified through tests.

It is ideal if the EMC knowledge of Langer EMV-Technik GmbH is already incorporated into your first development sample during the development process. You save development time thanks to ideal starting conditions. The knowledge gained can then be implemented directly in your own work area for further developments, which visibly increases the efficiency and quality of the development work.

Co-funded by the European Union

This project is co-financed from tax revenues on the basis of the budget adopted by the Saxon State Parliament.

LANGER EMV-Technik GmbH
Nöthnitzer Hang 31
01728 Bannewitz
Germany